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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,347	10/21/2003	Tiemin Zhao	38493-8017US1	6636

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/691,347	ZHAO ET AL.	
	Examiner	Art Unit	
	NHAN T. TRAN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,13-17,20-24 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,13-17,20-22,24,27-29 and 31* is/are rejected.

7)☒ Claim(s) *23 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/5/2008 have been fully considered but they are not persuasive.

The Applicants assert that the Examiner's assertion of the "whole circuit 1150" to read on a pull-down circuit is confusing and request for clarification. The Applicants also conclude that the claimed limitations are not anticipated by Pain (remarks, pages 6-7).

In response, the Examiner understands the Applicants' arguments and respectfully submits clarification on Pain's disclosure that meets all alleged claim limitations.

As shown in Fig. 11B of Pain, the pull-down circuit is indicated by circuit 1158 that implements a pull-down function during which the sensor potential is pulled down (hard reset as shown in Fig. 13 to pull down the sensor potential to a level lower than 2.4V prior to the soft reset). The reset voltage line is the voltage line connected between transistor 1152 and the drain 1104 of reset transistor connected to RST shown in Fig. 11B (note Fig. 11A for the drain 1104 that is not shown in Fig. 11B; see col. 6, line 61 - col. 7, line 25). Furthermore, the reset transistor RST is clearly coupled between the reset voltage line and the sensor (photodiode PD). In view of the above, the Examiner believes the interpretation of the claimed limitations reads on Pain's disclosure.

The Applicants further argue that the "Pix-Out" in Pain is not corresponding to the bit line used to pull down the sensor potential as required in claim 20 (remarks, pages 7-8).

In response, the Examiner understands the Applicants' argument but respectfully disagrees.

First of all, the bit line as claimed is not necessarily a part of "pull-down circuit." Rather, it appears in claim 20 that the bit line may be another circuit that also acts to pull down the sensor potential. In Pain, the "Pix-Out" clearly acts to pull down the sensor potential during reading out signal charges from the photodiode. Since the signal charges are readout from the photodiode PD through "Pix-Out", the sensor potential of the photodiode is pulled down by inherency of draining the charges. Secondly, although the combination of claims 1 and 20 require that the pull down is performed prior to the reset function (soft reset function as in Pain), this is still met by Pain in which the sensor potential is pulled down during the readout period of a first frame *prior to the soft reset period of a next frame* (please note that claim 20 does not require a specific timing within a frame period).

In view of the above, the broadest interpretation of the claimed limitations does read on Pain's disclosure. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 13-17, 20, 24, 27 & 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Pain et al. (US 6,721,464).

Regarding claim 1, Pain discloses an active pixel sensor circuit (Fig. 11B and col. 2, lines 40-47), comprising:

a sensor (photodiode PD) for producing a sensor potential (Fig. 11B and col. 6, lines 61-64);

a pull-down circuit (circuit 1158 in Fig. 11B) for implementing a pull down function during which the sensor potential is pulled down below a selected critical level (Fig. 13 and col. 6, line 61 – col. 7, line 25, wherein the sensor potential is pulled down to a hard-reset level by virtue of the hard-reset);

a reset voltage line (the voltage line connected between transistor 1152 and the drain 1104 of reset transistor connected to RST shown in Fig. 11B) coupled to the pull-down circuit; and a reset transistor (the transistor connected to RST line) coupled between the reset voltage line and the sensor (PD), wherein during the pull down function, the reset transistor is conducting and the pull-down

circuit operates to pull down the sensor potential below the selected critical level (see Fig. 13), the pull down function being performed prior to a reset function (soft-reset function) when the sensor potential is reset to a selected level (see col. 7, lines 5-25, wherein the reset function is considered as the soft-reset function which is subsequently performed after the hard-reset function).

Regarding claim 13, it is clear in Pain that the sensor comprises a photodiode (PD in Fig. 11B, see claim 1).

Regarding claim 14, Pain also discloses that the selected critical level is determined according to the potential at which the reset transistor will be on when the reset function (soft-reset) starts (see Fig. 13 and col. 7, lines 5-25).

Regarding claim 15, it is also seen in Pain that the timing of the pull down function is such that the sensor is stabilized at a level below the selected critical level before the reset function starts (Fig. 13 and col. 7, lines 5-25).

Regarding claims 16 & 17, these method claims are also met by the analyses of claims 1 & 15, respectively.

Regarding claim 20, it is also seen in Pain that the sensor is coupled through a plurality of transistors to a bit line (Pix-Out in Fig. 11B), and the bit line

is used to pull down the sensor potential (Figs. 11B-13 and col. 6, line 61 – col. 7, line 25 and note the Examiner's response in section 1 above).

Regarding claim 24, Pain discloses an active pixel sensor circuit in which a soft reset function is performed (Figs. 11B-13 and col. 6, line 61 – col. 7, line 25), the active pixel sensor circuit comprising:

a sensor (photodiode PD) which outputs a sensor potential (Fig. 11B and col. 6, lines 61-64);

a reset transistor (the transistor connected to RST line) coupled to the sensor; and a bit line (Pix-Out) coupled through a plurality of transistors to the sensor, wherein the sensor potential is pulled below a selected critical level (by virtue of hard-reset) prior to the time when a soft reset function is performed to reset the sensor potential (see Figs. 11B – 13 and col. 6, line 61 – col. 7, line 25). *It should be noted that the claimed "a bit line" does not necessarily function as a pull down circuit but it appears that the pull down is performed by something else in this claim.*

Regarding claims 27 & 31, these claims are also met by the analyses of claims 20 & 14, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 21-22, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. (US 6,721,464) in view of Krymski (US 6,917,027).

Regarding claim 21, although Pain teaches the bit line as discussed in claim 20, Pain does not explicitly disclose that a loading transistor is coupled to the bit line, and the voltage potential on the bit line is pulled down by increasing bias on the loading transistor.

However, it is well recognized by Krymski in Fig. 1 that the bit line (125) is coupled to a loading transistor (130, col. 2, line 23), wherein when the loading transistor is turned on by increasing the gate voltage at vln, the voltage potential on the bit line is pulled down to Vss (i.e., ground).

Therefore, it would have been obvious to one of ordinary skill in the art to configure the pixel circuit in Pain to include a loading transistor coupled to the bit line for pulling down the potential of the bit line by increasing the bias on the loading transistor so as to filter kTC noise as taught by Krymski, col. 1, lines 43-44.

Regarding claim 22, Pain in view of Krymski also teaches a biasing circuit (indicated by vln in Fig. 1 of Krymski), and the biasing circuit is used to increase the bias on the loading transistor.

Regarding claims 28 & 29, these claims are also met by the analyses of claims 21 & 22, respectively.

Allowable Subject Matter

4. Claims 23 & 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHAN T. TRAN whose telephone number is

(571)272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nhan T. Tran/
Primary Examiner, Art Unit 2622